IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Swoboda
Art Unit: 2123
Serial No.: 09/483,570
Examiner: Thai Q. Phan
Filed: January 14, 2000
Docket: TI-28933
For: SOFTWARE EMULATION MONITOR EMPLOYED WITH HARDWARE SUSPEND MODE

Appeal Brief under 37 C.F.R. §1.192

CERTIFICATION OF FAX TRANSMITTAL
UNDER 37 C.F.R. §1.6(b)

I hereby certify that the above correspondence is being facsimile transmitted to the Patent and Trademark Office on December 31, 2003.

Robin E. Barnum

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This is Appellant's Appeal Brief filed pursuant to 37 C.F.R. §1.192 and the Notice of Appeal filed October 31, 2003.

Real Party in Interest under 36 C.F.R. §1.192(c)(1)

The real party in interest in this application is Texas Instruments Incorporated, a corporation of Delaware with its principle place of business in Dallas, Texas. An assignment to Texas Instruments Incorporated is recorded at reel 010509 and frames 0247 and 0248.

Related Appeals and Interferences under 36 C.F.R. §1.192(c)(2)

There are no appeals or interferences related to this appeal in this application.

Status of the Claims on Appeal under 37 C.F.R. §1.192(c)(3)

The claims are 1, 3 and 4. Claim 2 has been canceled. Claims 1, 3 and 4 are finally rejected. No claims are allowed.

Status of Amendments Filed After Final Rejection under 37 C.F.R. §1.192(c)(4)

The response filed September 30, 2003 after the FINAL REJECTION of August 1, 2003 proposed no amendments to the claims.

Summary of the Invention under 37 C.F.R. §1.192(c)(5)

This invention is a method of in circuit emulation of an integrated circuit. The integrated circuit includes a digital data processor capable of executing program instructions and a serial scan path for control of the state of the integrated circuit. The method detects a predetermined debug event. Upon detection of such a predetermined debug event, the method suspends program execution except for at least one type interrupt. The method executes an emulation monitor program via this interrupt. The method selectively assigns control of the at least one emulation resource to the serial scan path or the monitor program.

Two methods are disclosed for assigning the emulation resource. When the integrated circuit includes a monitor privilege input, the emulation resources may be assigned to the serial scan path upon a first digital state of the monitor privilege input and to the emulation monitor program upon a second digital state of the monitor privilege input. When the integrated circuit includes at least one read write data register, assignment of the emulation resources includes accessing the read write data register.

Statement of Issues Presented for Review under 37 C.F.R. §1.192(c)(6)

Are claims 1, 3 and 4 made obvious under 35 U.S.C. 103(a) by the combination of Itoh et al U.S. Patent No. 6,075,941 and Sample et al U.S. Patent No. 5,960,191?

Statement of the Grouping of Claims under 37 C.F.R. §1.192(c)(7)

The Applicants respectfully submit that the claims of this application are independently patentable in the following groups:

Group I: claim 1;

Group II: claim 3; and

Group III: claim 4.

This Appeal Brief includes separate arguments for each of these groups. In accordance with the procedure sanctioned in MPEP §1206(5) the Appellant respectfully submits these separate arguments fulfill the requirement of 37 C.F.R. §1.192(c)(6) for statement of the reason why the claims are believed separately patentable.

Arguments

Group I

Claim 1 recites subject matter not made obvious by the combination of Itoh et al and Sample et al. Claim 1 recites "selectively assigning control of at least one emulation resource of the integrated circuit to one of said serial scan path or said monitor program." The FINAL REJECTION states at page 3, lines 12 to 14:

> "Itoh does not expressly disclose selectively assigning control of at least emulation resource of the integrated circuit to one of the serial scan path or the emulation program as claimed."

The FINAL REJECTION cites Sample et al to teach this limitation. The FINAL REJECTION states at page 3, lines 14 to 18:

> "In fact, Sample (patent 5,960,191) teaches method and system for hardware emulation system including feature of selectively assigning control of emulation resource for circuit emulation system (col. 3. lines 35-49, col. 19, line 48 to col. 24, line 4) and serially scanning path for emulation resource assignment resources as taught in Background of the Invention."

The Applicants respectfully submit that the technique taught in Sample et al so differs from the claimed subject matter that the claimed subject matter is unobvious.

First, Sample et al is directed to a different problem than that claimed. Claim 1 recites a method of "in circuit emulation." This application states at page 3, line 25 to page 4, line 6:

> "Product development and debugging is best handled with an emulation circuit closely corresponding to the actual integrated circuit to be employed in the final product. In circuit emulation (ICE) is in response to this need. An integrated circuit with ICE includes auxiliary circuit not needed in the operating product included solely to enhance emulation visibility. In the typical system level integration circuit, these emulation circuits use only a very small fraction of the number of transistors employed in operating circuits. Thus it is feasible to include ICE circuits in all integrated circuits manufactured. Since every integrated circuit can be used for emulation, inventory and manufacturing need not differ between a normal product and an emulation enhanced product."

This portion of the application teaches that in circuit emulation includes circuits manufactured on every integrated circuit used for product development and debugging. In contrast, Sample et al teaches hardware emulation systems for a different purpose. Sample et al states at column 1, lines 11 to 16:

> "Hardware emulation systems are devices designed for verifying electronic circuit designs prior to fabrication as chips or printed circuit boards. These systems are typically built from programmable logic chips (logic chips) and programmable interconnect chips (interconnect chips)."

Verification during circuit design cannot involve in circuit emulation which include circuits in every manufactured integrated circuit. The teachings of Sample et al are applicable to integrated circuit design and not to product development and debugging. Thus any teaching of Sample et al is inapplicable to this invention.

Second, the teaching of Sample et al do not make obvious the particular selectively assigning control of claim 1. Sample et al states at column 1, line 66 to column 2, line 12:

> "Time-multiplexing is a technique that has been used for sharing a single physical wire or pin between multiple logical signals in certain types of systems where the cost of each physical connection is very high. Such systems include telecommunication systems. Time-multiplexing, however, has not been commonly used in hardware emulation systems such as those available from Quickturn Design Systems, Inc., Mentor Graphics Corporation, Aptix Corporation, and others because the use of prior art time-multiplexing methods significantly reduced the speed at which the emulated circuit could operate. Furthermore, prior art time-multiplexing techniques makes it difficult to preserve the correct asynchronous behavior of an embedded design in the hardware emulation system."

Thus Sample et al teaches his time-multiplexing technique is directed to sharing multiple logical signals on a single physical line. Sample et al fails to teach or suggest that the emulation resources shared on a time basis are selectively assigned to the serial scan path or the emulation monitor as recited in claim 1 Thus Sample et al teaches reassignment of emulation resources in a different context and for a different purpose than claimed. Sample et al fails to teach or suggest the selective assignment claimed.

Accordingly, claim 1 is allowable over the combination of Itoh et al and Sample et al.

Neither Itoh et al nor Sample et al include any teaching of the serial scan path recited in claim 1. The serial scan path as recited in this application has a meaning in the art. This application teaches at page 5, lines 11 to 13 this serial scan path corresponds to standard IEEE 1149.1, also known as JTAG (page 8, lines 23 to 25). Itoh et al teaches peripheral 4 illustrated in Figure 1 as a "serial input/output circuit" at column 5, lines 41 to 34. Sample et al includes teaching of serial data encoding. Neither of these "serial" references of Itoh et al and Sample et al deal with the structure recited in claim 1. Accordingly, claim 1 is unobvious over the combination of Itoh et al and Sample et al.

Paragraph 5 of the ADVISORY ACTION of October 10, 2003 states "the argued feature of 'the emulation resources shared on a time basis are selectively assigned to the serial scan path or the emulation monitor' is not present in the claim before for consideration." The Applicant disputes this assertion. Claim 1 recites "selectively assigning control of at least one emulation resource of the integrated circuit to one of said serial scan path or said monitor program." This application teaches at page 5, lines 15 to 18 and claim 4, that this assignment includes accessing the data register. The Applicant respectfully submits that one skilled in the art would recognize that such accessing the data register could take place on a time basis as previously argued.

Group II

Claim 3 recites subject matter not made obvious by the combination of Itoh et al and Sample et al. Claim 3 recites "said step of selectively assigning emulation resources of the integrated circuit assigns said emulation resources to said serial scan path upon a first digital state of said monitor privilege input and

assigns said emulation resources to said emulation monitor program upon a second digital state of said monitor privilege input." This recitation requires the assignment of the emulation resource based upon the state of a monitor privilege input. The FINAL REJECTION states at page 4, lines 3 to 5:

> "As per claim 3, Itoh discloses monitor program for monitoring priority interrupt, which could include privilege input for monitor program, monitoring privilege interrupt input for the and assigning resources for emulation program and path tracing circuit."

The Applicant respectfully submits that this is not evidence of obviousness but mere conjecture. Itoh et al discloses a monitor program begun as a result of a debug interrupt. Itoh et al fails to teach that assignment of an emulation resource is dependent upon a "privilege input for monitor program." Indeed, Itoh et al fails to teach such a "privilege input for monitor program." The FINAL REJECTION fails to state that Itoh et al discloses such an input or where it discloses such an input. The FINAL REJECTION merely states that such an input is possible. In the absence of any teaching with the reference of this input or of the claimed function of this input, claim 3 is allowable over the combination of Itoh et al and Sample et al.

Group III

Claim 4 recites subject matter not made obvious by the combination of Itoh et al and Sample et al. Claim 4 recites "said step of selectively assigning emulation resources of the integrated circuit includes accessing said at least one read write data register." The FINAL REJECTION states at page 4, lines 6 to 8:

"As per claim 4, Itoh discloses emulation resources and accessing to the emulation resources through read/write data register (Figs. 3-20, col. 8, lines 26-59, cols. 9-13, for example)."

Itoh et al teaches registers: debug control register (0) 21; debug control register (1) 22; address comparison register (0) 23; address comparison register (1) 24; data comparison register 25; and debug register 26. These are indeed emulation resources that are read/write data registers that can be accessed by CPU 1. However, the portion of Itoh et al cited in the FINAL REJECTION fails to teach that the claimed "selectively assigning control of at least one emulation resource of the integrated circuit" either to the serial scan path or the emulation monitor (per claim 1) includes accessing a data register. While Itoh et al teaches that emulation operations can be changed by accessing these data registers, it fails to teach the claimed selectively assigning. Accordingly, claim 4 is allowable over the combination of Itoh et al and Sample et al.

If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicants' attorney at the below listed telephone number and address to facilitate prosecution.

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Respectfully submitted,

Robert D. Marshall, Jr.
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APPENDIX

CLAIMS ON APPEAL

1. A method of in circuit emulation of an integrated circuit including a digital data processor capable of executing program instructions, the integrated circuit including a serial scan path for control of the state of the integrated circuit, comprising the steps of:

detecting a predetermined debug event;

upon detection of said predetermined debug event suspending program execution except for at least one type interrupt;

executing an emulation monitor program via said at least one type interrupt; and

selectively assigning control of at least one emulation resource of the integrated circuit to one of said serial scan path or said monitor program.

3. The method of claim 1, wherein the integrated circuit includes a monitor privilege input, said method wherein:

said step of selectively assigning emulation resources of the integrated circuit assigns said emulation resources to said serial scan path upon a first digital state of said monitor privilege input and assigns said emulation resources to said emulation monitor program upon a second digital state of said monitor privilege input.

4. The method of claim 1, the emulation resources include at least one read write data register, said method further comprising:

said step of selectively assigning emulation resources of the integrated circuit includes accessing said at least one read write data register.

To: Technology Center: 2123
Facsimile Number: 703-872-9306

Total Pages Sent: 12

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of Gary L. Swoboda
Serial No.: 09/483,570
Filed: January 14, 2000
For: Software Emulation Monitor Employed With Hardware Suspend Mode

TI-28933
Art Unit: 2123
Examiner: Thai Q. Phan
Conf. No.: 8552

CERTIFICATION OF FACSIMILE TRANSMISSION

I hereby certify that the following papers are being transmitted by facsimile to the U.S. Patent and Trademark Office at 703-872-9306 on the date shown below:

Robin E. Barnum

December 31, 2003
Date

FACSIMILE COVER SHEET

X FACSIMILE COVER SHEET	___ AMENDMENT (# Pages)
___ NEW APPLICATION	___ EOT (# Pages)
___ DECLARATION (# Pages)	___ NOTICE OF APPEAL (Page)
___ ASSIGNMENT (# Pages)	X APPEAL Brief (10 Pages)
___ FORMAL DRAWINGS	___ ISSUE FEE (# Pages)
___ INFORMAL DRAWINGS	___ REPLY BRIEF (IN TRIPLICATE) (# Pages)
___ CONTINUATION APP'N (# Pages)	X Appeal Brief Fee TL (1 page)
___ DIVISIONAL APP'N	

NAME OF INVENTOR(S): Gary L. Swoboda	RECEIPT DATE & SERIAL NO.: **Serial No.: 09/483,570** **Filing Date:** January 14, 2000
TITLE OF INVENTION: Software Emulation Monitor Employed With Hardware Suspend Mode	
TI FILE NO.: **TI-28933** / DEPOSIT ACCT. NO.: **20-0668**	
FAXED: 12/31/03 DUE: 12/31/03 ATTY/SEC'Y: RDM/reb	

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NOTICE OF APPEAL FROM THE PRIMARY EXAMINER TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

Attorney Docket No. TI-28933

#11 no. A
11-7-03

In re application of:

Gary L. Swoboda

Serial No.: 09/483,570

For: Software Emulation Monitor Employed With Hardware Suspend Mode

Filed: January 14, 2000

Conf. No.: 8552

Group Art Unit: 2123

To: Commissioner for Patents

Sir:

Applicant hereby appeals to the Board of Patent Appeals and Interferences from the decision in the Office Action dated August 1, 2003 and the Advisory Action dated October 10, 2003 of the Primary Examiner finally rejecting Claims 1, 3 and 4. The item(s) checked below are appropriate:

1. __ An extension of time to respond to the final rejection
   - __ was granted on
   - __ is requested for ___ month - see attached copy.
2. X A timely response to the final rejection has been filed, as provided in 841 O.G. 1411.
3. X Fee $330.00:
   - __ Not required (*Fee paid in prior appeal*)
   - X The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment to Texas Instruments Incorporated, Deposit Account No. 20-0668

11/07/2003 THALL1 00000001 200668 09483570
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Signature [Rule 191(b)]

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